CLAIMS:

What is claimed is:

1. A high speed static multiplexer comprising:

a plurality of data inputs and at least one select input;

an output;

a high voltage rail and a low voltage rail;

a pull-up circuit coupled between said output and said high voltage rail and further coupled to said plurality of data inputs and said at least one select input, wherein said pull-up circuit generates a first logic state at said output in response to a selected data input having said first logic state; and

a pull-down circuit coupled between said output and said low voltage rail and further coupled to receive said plurality of data inputs and said at least one select input, wherein said pull-down circuit generates a second logic state at said output in response to a selected data input having said second logic state.

2. The high speed static multiplexer of Claim 1, wherein said pull-up circuit comprises:

a P-type transistor having a control node, and a first and second data node, coupled at said first data node to said output and at said second data node to said high voltage rail, wherein said P-type transistor exhibits signal swings less than said high voltage rail;

a plurality of N-type transistors, each having a control node, and a first and second data node, wherein said second data node of each of said plurality of N-type transistors is coupled to a control node of said P-type transistor, said first data node of each of said

plurality of N-type transistors is coupled to a respective one of said plurality of data inputs, and said control node of each of said plurality of N-type transistors is coupled to said at least one select input.

3. The high speed static multiplexer of Claim 2, wherein said pull-down circuit comprises:

a plurality of sets of N-type transistors, wherein each set includes a first and second transistor coupled in series, and further wherein said second transistor is coupled at its second data node to said low voltage rail and at its control node to one of said at plurality of data inputs, and wherein said first transistor is further coupled at its control node to said at least one select input and at its first data node to said first data node of said P-type transistor.

4. The high speed static multiplexer of Claim 1, wherein each of said plurality of inputs are coupled to a respective inverter.

5. A high-speed static multiplexer comprising:

at least two data inputs circuits that each receive a respective data input;

at least one select input, wherein each of said at least one select input receives a respective select signal;

an output; and

a plurality of transistors operationally coupled between said at least two data input circuits and said output, wherein said plurality of transistors each have a control node and a first and second data node and wherein said plurality of transistors are controlled by both data inputs and select signals to select of one of said data inputs to yield said output.

6. The high speed static multiplexer of Claim 5, wherein said plurality of transistors include a P-type transistor and a plurality of sets of first, second, and third N-type transistors for each of said at least two data inputs.

7. The high-speed static multiplexer of Claim 6, wherein each of said at least two data input circuits includes an in-line inverter for inverting said respective data input to produce an inverted input.

8. The high speed static multiplexer of Claim 7, wherein:

each of said at least two data input circuits is coupled to a control node of said third N-type transistor and to a first data node of said first N-type transistor; and

said at least one select signal input is coupled to a control node of said first N-type transistor and to a control node of said second N-type transistor;

9. The high speed static multiplexer of Claim 8, wherein further:

a second data node of said first N-type transistor is connected to a control node of said P-type transistor;

a second data node of said P-type transistor is connected to a power supply (V_{DD}); and

a first data node of said P-type transistor is connected to said output.

10. The high speed static multiplexer of Claim 9, wherein further:

a second data node of said third N-type transistor is connected to ground;

a first data node of said third N-type transistor is coupled to a second data node of said second N-type transistor; and

a first data node of said second N-type transistor is coupled to said first data node of said P-type transistor at said output.

11. The high speed static multiplexer of claim 6, wherein said P-type transistor has an on state and off state and wherein a voltage differential at said control node to change between said on and off states is less than the voltage differential between a high voltage applied at a second data node of said P-type transistor and a low voltage applied at a second data node of said third N-type transistor.

12. The high speed static multiplexer of claim 6, wherein said plurality of transistors are field effect transistors (FETs).

13. A multi-level high-speed static multiplexer comprising:

a plurality of connected levels of high speed static multiplexers, wherein each of said high speed multiplexers comprises:

a plurality of data inputs and at least one select input;

an output;

a high voltage rail and a low voltage rail;

a pull-up circuit coupled between said output and said high voltage rail and further coupled to said plurality of data inputs and said at least one select input, wherein said pull-up circuit generates a first logic state at said output in response to a selected data input having said first logic state; and

a pull-down circuit coupled between said output and said low voltage rail and further coupled to said plurality of data inputs and said at least one select input, wherein said pull-down circuit generates a second logic state at said output in response to a selected data input having said second logic state; and

wherein each of said outputs at a first level of said plurality of levels is coupled to one of said plurality of data inputs of said high speed static multiplexers at a next level of said plurality of levels, wherein a multiplicative-input multiplexer is realized having NxM possible outputs, where N is a number of data inputs at said first level and M is the number of data inputs at the next level.

14. The multi-level high speed static multiplexer of Claim 13, wherein said plurality of levels includes more than two levels with a final level having a single high speed static multiplexer, and wherein each of said outputs of a given level is fed into at least one input at a next level until said final level.

15. The multi-level high speed static multiplexer circuit of Claim 14, wherein each even number of levels yields a corrected output and each odd number of level yields an inverted output.

16. The multi-level high speed static multiplexer of Claim 15, further comprising an inverter coupled to each of said data inputs at said first level when said number of levels is odd.

17. The multi-level high speed static multiplexer of Claim 15, further comprising an inverter coupled to said output at said final level when said number of levels is odd.